Latent Damage in CMOS Devices from Single-Event Latchup

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Abstract:

Latent damage effects from single-event latchup are studied, revealing a previously unconsidered reliability hazard for CMOS devices. Several device types were found to remain functional despite significant structural damage to their interconnects from SEL.

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I. Introduction

Radiation effects on microelectronics are an important reliability issue for many space applications. In particular, single-event latchup (SEL) susceptibility is often considered sufficient reason to not use a device in space. However, latchup sensitive devices are sometimes flown in conjunction with mitigation hardware or software. For this reason, it is important to know the behavior of such devices during latchup in order to effectively circumvent failure. This study discusses recently observed latent damage effects from SEL. Latent damage was observed in multiple CMOS device types and represents a possible reliability hazard that previously has not been considered.

A previous study of Analog Device's AD9260 described the initial observation of catastrophic and latent structural damage from SEL during heavy ion and laser testing [1]. The results of that study created an interest in investigating similar behavior in a broad range of CMOS devices.

This paper discusses results for several device types that remained functional despite significant structural damage to their interconnects from SEL. A full description of the characteristic physical signatures of latent damage is included, along with key parameters of these types of events. An explanation of why some structurally damaging latchup events are non-catastrophic is presented, along with the threshold current density for damage.

II. Experimental

A. Test Methods

Six types of CMOS devices were studied for SEL-induced structural damage. All device types experienced catastrophic structural damage, but three types also exhibited "latent damage"- structural damage that did not cause device failure. Table 1 lists the studied devices and their susceptibility to latent damage determined to date.

The AD9260 was tested at The Aerospace Corporation's laser facility. A Hewlett-Packard 6629 power supply provided voltage to delidded test devices mounted on a manufacturer-supplied evaluation board.

The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program (NEPP), Code AE.

Table 1. CMOS Devices Studied for SEL-induced damage.

CMOS Device	Device Type	Manufacturer	Latent Damage
AD9260	ADC	Analog Devices	Yes
AD9240	ADC	Analog Devices	No
ADC10321	ADC	NSC	Yes
CAR/CPPX1T-A7BR	Oscillator	Cardinal/Cypress Hybrid	Yes
LTC1799	Oscillator	Linear Technology	No
ADSP2100	DSP	Analog Devices	No

Supply currents were measured during latchup events through a 1-ohm sampling resistor and a differential pre-amplifier made by Tektronix. SEL events were recorded as waveforms in a digital oscilloscope and analyzed via computer software. The devices were irradiated with single 815nm, 1nJ laser pulses with a 3-4μm spot size and a 10ps pulse width. The power supply to the DUT was turned on 10ms before each laser pulse and remained on for 1ms after the pulse. Device functionality was monitored with an oscilloscope. The position of the laser spot was monitored with a viewing screen linked to a CCD camera focused on the devices. This monitoring system was also used after every laser pulse to determine if latent damage had occurred.

The 5 additional CMOS device types listed in Table 1 were tested for latent damage in vacuum at room temperature, using a californium fission fragment source at JPL to induce latchup. The same current waveform and DUT functionality monitoring technique was used, but did not provide direct information about latent damage. The time that SEL equilibrium supply currents were held before power to the DUT was clamped varied among device types. The RC time constant changed due to differing amounts of capacitance on the evaluation boards.

B. Diagnostic Approach

Because of the random location of the fission fragments, latchup testing at JPL's ^{252}Cf facility did not allow direct observation of the region on the device where we were causing latchup-induced damage. This necessitated simultaneous monitoring of the SEL equilibrium current and device functionality one event at a time. After a latchup event, the DUT was removed from the vacuum chamber, and the die was scanned with an optical microscope for potential damage sites. These sites usually appeared as round, shiny regions relative to surrounding material. If

damage was suspected, the device was evaluated using scanning electron microscopy (SEM). SEM allowed us better resolution and the ability to perform Energy Dispersive Spectroscopy where the x-ray spectra of the damage site was matched against the characteristic spectra of various elements.

In order to determine the feature sizes of damaged interconnects and more clearly observe the structural damage to the metal, plasma etching or acid stripping was used to remove the top layer of insulator material from the die. All of the studied devices were aluminum/Si_3N_4 or aluminum/SiO_2 systems with 2-3 levels of metal clad with TiN or TiW refractory metal. Metallization thicknesses ranged from 1.0-1.2μm.

III. RESULTS

A. Latent Damage Signatures

Several latent damage signatures emerged that were common to all the device types tested. The round, shiny regions observed optically were found to be spheres of aluminum near significantly voided interconnects. The insulator material surrounding damaged interconnects was often cracked and sometimes fractured and lifted to release metal from underneath. Latent damage most often occurred in the top level of metal, and all tested devices of the same part type were damaged in the same area on the die.

Figure 1 shows several of these signatures. The three extruded aluminum spheres in the left interconnect created a voided region directly above them. This damage occurred in the top level of metal.

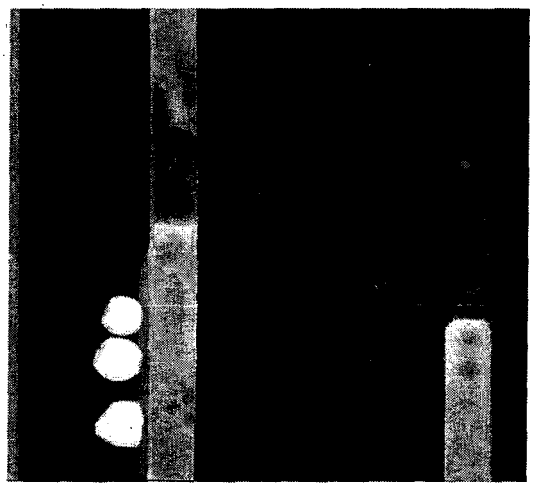

Fig. 1 Scanning electron micrograph of latent damage in an AD9260 with nitride removed.

Figure 2 shows cracked and lifted insulator material at the site of an erupted metal sphere on a latently damaged National ADC10321.

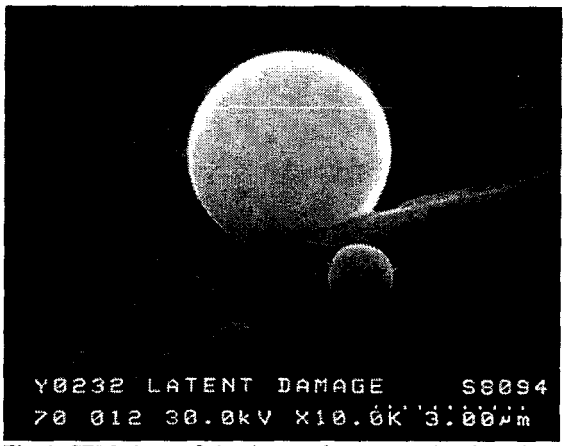

Fig. 2 SEM photo of aluminum spheres emerging from fractured and lifted insulator on a latently damaged National ADC10321.

Although one incidence of metal damage in a contact region was observed in the Cypress oscillator, damage associated with vias where metallization may have had smaller dimensions was not a trend that we observed.

B. Key Parameters of Latent Damage

A minimum current density of 10^7A/cm^2 was necessary to produce latent damage in the studied devices. The range of current densities observed for the three device types that exhibited latent damage was approximately 10^7-10^8A/cm^2. These numbers are based on the latchup equilibrium current drawn by the DUT and the cross-sectional area of the damaged interconnect determined during post-test SEM evaluation. The cross-sectional areas of damaged interconnects ranged from 1-10μm^2. Damaging latchup event durations ranged from 60μs to 18ms. A graph illustrating the current densities and event durations associated with particular device types is presented in the analysis section of the summary.

IV. ANALYSIS

A. SEL-Induced Damage Mechanism

Interconnect failures from high current pulses have often been studied using simple test structures with feature sizes and insulator thicknesses similar to those of the CMOS devices studied in this paper [2-8]. A study by Banerjee et al.[2] of a 4-level metal system subjected to 200ns high current pulses reported open circuit failure and melting of the interconnects in the test structures at current densities of approximately $5x10^7$A/cm^2 for metal 4 and $6x10^7$A/cm^2 for metal 1-3. Melting was due to resistance increases and corresponding temperature increases within the interconnects of over 1000°C. The events occurred

over a long enough duration to be considered steady state and subject to a certain degree of heat dissipation. The study also found that the maximum allowable current density decreased with increasing pulse width.

Our SEM evaluation of damage sites, the magnitudes of damaging current densities, and damaging event durations suggest that a similar mechanism is causing SEL-induced structural damage. High current densities during SEL cause temperature increases in interconnects which lead to melting of metallization and stresses caused by the mismatched thermal expansion coefficients of the metal and insulator material that comprise the line [3]. This stress causes cracking of the insulator which allows melted metal to erupt from the line, often to the point of catastrophic voiding. As the extruded metal cools, it forms into a sphere, the most spacially efficient shape.

B. Rationale for Latent Damage

Interestingly, our data on the current densities and event durations involved for non-destructive latchup events correspond to conditions for failure indicated by previous studies using electrical pulses [2,4-5]. Figure 3 shows latent damage data for the AD9260, National's ADC10321, and the Cardinal/Cypress oscillator. For comparison, we show the data for interconnect failures from Ref. 2 and 4. What is striking is that our current densities are higher and our pulse widths longer than those predicted for failure, and yet we are seeing only latent damage in many devices.

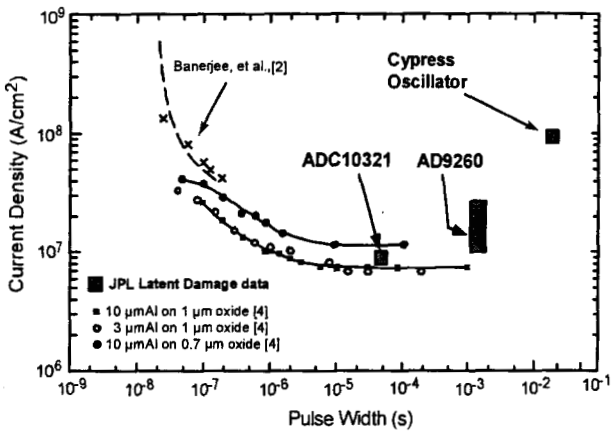

Figure 3. Latent Damage data compared with conditions for interconnect failure from studies in Ref.'s 2 and 4.

Our SEM analysis suggests several reasons why some damaging latchup events are not catastrophic. The amount of released metal may simply be too small to cause complete interconnect voiding and device failure. Another possibility is that barrier metal between the aluminum and insulator material may remain intact after voiding of the aluminum in some interconnects. This cladding may maintain electrical continuity [9] following a damaging SEL event. The latently damaged device in Fig. 1 could have remained functional for this reason (note the thin "rails" that bridge the voided region).

More dramatically, after melting and re-crystallization, some metal may form a bridge across the void, keeping the circuit closed and causing only non-catastrophic damage. This is illustrated in Figure 4. However, the interconnect cross-section in the damaged region may be significantly smaller than originally intended for normal operating conditions and more susceptible to later failures, either from subsequent latchup events or electromigration.

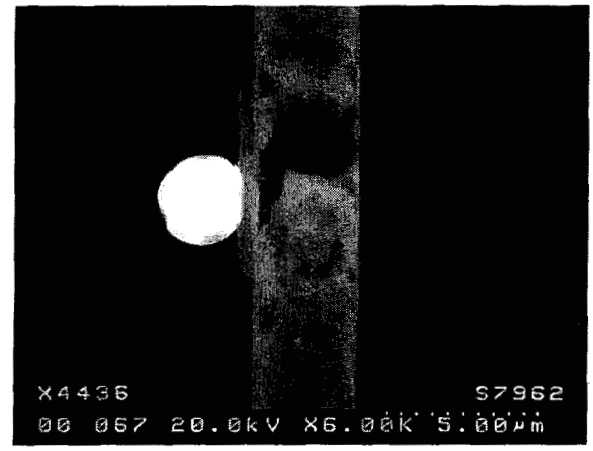

Figure 4. A latently damaged AD9260 interconnect with an aluminum "bridge" across a void.

V. DISCUSSION

A. Reliability Issues

The latent damage effects from SEL presented in this paper introduce a reliability hazard that has not been studied previously. Figures 1 and 4 show that SEL can cause interconnect cross-sections to be reduced by approximately 1 to 2 orders of magnitude without affecting DUT functionality. The resistance increase caused by these smaller cross-sections can potentially increase failure from subsequent latchup events where current densities would be expected to be even higher than before latent damage occurred.

Vulnerability to electromigration damage is another concern. Localized melting and re-crystallization of metal lines can result in a reduction of grain size and the creation of a larger number of grain boundaries in the lines [6]. This can exacerbate electromigration-related damage, and may contribute to long-term

reliability problems for parts that have sustained SEL-induced latent damage.

An additional danger is introduced for devices that do not have encapsulating plastic packaging, such as the ceramic packaging of the ADSP2100 where an air gap exists between the chip and a metal lid. If metal spheres from latent damage were to become dislodged and mobile due to vibration or a low-gravity environment, they could potentially cause a short circuit by coming in contact with other wiring.

B. Effect on Future SEL Mitigation Efforts

This paper shows that SEL-induced latent damage is not an isolated incident associated with only one CMOS device type. Three of the 6 device types studied to date have shown latent damage, indicating that it may be a pervasive problem.

Our first observation of SEL-induced structural damage was during laser testing, which allowed direct, microscopic observation of the delidded DUT. Such monitoring would not have been possible at an accelerator facility. Since latent damage causes no obvious change in device functionality, we would not have known that latently damaging SEL's had occurred at an accelerator unless subsequent surface analysis were done. Efforts to design hardware or software for latchup mitigation should include considerations for possible latent damage events which may be hard to observe and may take place over very short time periods. As the study by Banerjee et al. illustrated, such damage can occur in under 200ns.

Typically, the goal of SEL testing for mitigation circuit design is to avoid failure so that the latchup cross section can be measured. A test circuit that includes some SEL detection and power clamping is usually used, and a histogram of the distribution of SEL current levels is generated. This method may overlook quickly occurring latent damage events that may not be mitigated by the final design.

C. Next-Generation Devices

The evolution of devices and processing technologies since the early 1980's has resulted in smaller feature sizes and increased numbers of levels of metal [9]. For a given current density, modeling has shown that, for multi-level systems, the top level of metal experiences the highest temperature increase, and this temperature increases as more levels of metal are used [7]. One possible reason for this is the relative distance from the silicon substrate heat sink [8]. The trend toward smaller feature sizes and even more densely packed levels of interconnects is expected to continue. Therefore, next generation devices may have a higher incidence of the type of SEL-induced latent damage presented in this paper.

VI. CONCLUSIONS

This summary demonstrates that for a variety of CMOS devices, single-event latchup may produce non-catastrophic interconnect damage from melting. Because this type of structural damage is permanent and significantly reduces interconnect cross-sections in the damaged area, it raises a concern about vulnerability to future device failure due to electromigration or additional SEL events. Latchup circumvention efforts should take this type of damage into account, especially since it often occurs over very short time periods and is difficult to observe. Next generation devices are expected to contain smaller interconnects and more levels of metallization, and therefore may be more susceptible to this type of latent damage. Small ejected metal spheres emerged as a signature for identifying this type of damage. Reliability data in the literature and our test results show that the threshold current density for damage is $10^7 A/cm^2$.

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